Heterogeneous Integrated Microsystems With Nontraditional Through-Silicon Via Technologies

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(Invited Paper)

***Abstract*— In this paper, the design, fabrication, and high-frequency characterization of three types of nontraditional through-silicon via (TSV) technologies are discussed. First, the integration of TSVs within a silicon microfluidic heat sink is presented; TSVs are fabricated within a pin-fin heat sink, and the frequency response of TSVs within a deionized-water-filled silicon pin-fin heat sink is experimentally analyzed. Second, to electrically shield the signal transmission of such TSVs, coaxially shielded TSVs consisting of multiple ground TSVs surrounding a single signal TSV are demonstrated. It is experimentally shown that as the number of ground TSVs increases, shielding is improved. Finally, a partial air-isolation technique is proposed to reduce TSV loss and capacitance at high frequencies.**

***Index Terms*— 3-D microsystem, air isolation, coaxial through-silicon via (TSV), microfluidic cooling, microfluidic pin-fin, packaging, silicon microsystem.**

I. Introduction

DEMAND for high-bandwidth communication with low energy consumption continues to grow in modern computing systems [1], [2]. Through innovations in materials, processes, and structures, integrated circuit technology has rapidly evolved—transistor count has increased by a factor of 16 000, and gate speed has increased by a factor of 100 since the mid-1980s [2], [3]. Along with such efforts, the need for revolutionary innovation in system integration has become necessary to overcome the limitations of traditional packaging [4]. Moreover, chip-to-chip communication has emerged as a key bottleneck that limits total system performance. To address these needs, heterogeneous integrated microsystems in which multiple (and differing) dice are integrated within a single package have been proposed [5], [6]. Some of the proposed integrated microsystems include the vertical stacking of dice, i.e., 3-D integration, and the side-by-side bonding of chips on a substrate with dense interconnects, termed 2.5-D integration.

Manuscript received August 22, 2016; revised December 29, 2016; accepted February 9, 2017. Date of publication March 29, 2017; date of current version April 18, 2017. Recommended for publication by Associate Editor S. G.-Talocia upon evaluation of reviewers' comments.

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Digital Object Identifier 10.1109/TCPMT.2017.2678461

Through-silicon vias (TSVs) are a key enabler for stacked microsystems, providing vertical interconnection between stacked dice. The advantages of TSVs include high-bandwidth communication with greatly reduced routing lengths between dice. Moreover, they contribute to system miniaturization by geometrically integrating dice within the same footprint. For these reasons, TSV technology has been adopted in a number of applications that include CMOS image sensors (CISs), which are representative high volume-manufactured application [7], [8]. In addition, the dynamic random access-memory (DRAM) market continues to showcase the adoption of TSV technology in high-bandwidth memory [9], Wide-I/O DRAM [10], and hybrid memory cube [11] microsystems.

From the above-mentioned discussion, it is clear that TSV technology has been the focus of significant recent research, including studies that seek to improve the electrical and/or thermomechanical performance of TSVs by including atypical materials in a CMOS process flow or atypical configurations. In this paper, we refer to such TSVs as nontraditional TSVs. First, the integration of microfluidic cooling with TSVs has been proposed for various heterogeneous integrated microsystems [12]–[19]. Thermal management is one of the critical issues for 3-D integrated microsystems because they can exhibit relatively large heat flux [20]. With its effective cooling capability, microfluidic cooling has been explored as a promising solution to heat rejection. Recently, the monolithic integration of microfluidic cooling on the back side of a field-programmable gate array has been demonstrated, and measurements suggest improved performance compared to air cooling [13]. Moreover, coaxial TSV configurations have been explored to electrically shield signal vias from the surrounding medium [21]–[26]. A coaxial TSV structure consists of a center core via surrounded by an outer ground conductor. To fabricate this TSV configuration, several approaches have been explored, including polymers defined by photolithography [21], [24], organic material defined by laser ablation [22], [23], and silicon dioxide deposited by subatmospheric chemical vapor deposition (SACVD) [25]. Finally, low-loss TSV technologies have been explored to reduce electrical loss and capacitance resulting from a lossy silicon substrate. Various loss reduction techniques have been proposed, such as low-k liners, increased liner thickness [27], glass substrate [28], a localized

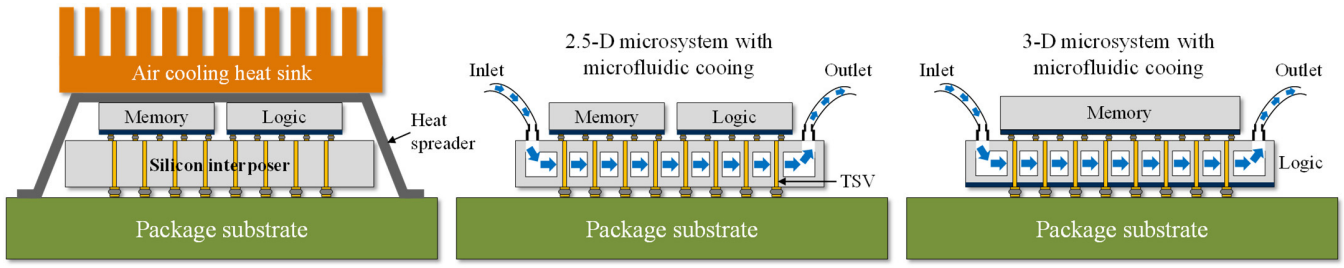


Fig. 1. Three types of heterogeneous integrated microsystems. (a) 2.5-D integration using silicon interposer with conventional air cooling technology. (b) 2.5-D integration using silicon interposer with embedded microfluidic cooling technology. (c) 3-D integration with embedded microfluidic cooling technology.

TABLE I
COMPARISON OF TSVs INTEGRATED WITH MICROFLUIDIC COOLING TECHNOLOGY

Parameters	C. R. King et al. [12]	Y. Madhour et al. [15]	N. Khan et al. [17]	Y. Zhang et al. [18]	H. Oh et al. [19]
TSV diameter	50 μm	60 μm	150 μm	13 μm	13 μm
TSV height	~300 μm	380 μm	400 μm	300 μm	320 μm
TSV pitch	200 μm	~200 μm	500 μm	24 μm	200 μm
Heat sink type	Channel	Channel	Channel	Pin-fin	Pin-fin
Heat sink width (or diameter)	100 μm	100 μm	50 μm	150 μm (diameter)	50, 100, 150 μm (diameter)
Heat sink height	200 μm	100 μm	175 μm*	200 μm	220 μm
Note	Long microchannel used	Vertical stack of 5 chips using solder bond	TSVs are not fabricated inside a heat sink	16 TSVs fabricated in each micropin-fin	TSV pitch is fixed for all diameters

*Two wafers are face-to-face bonded, so it gives a total height of 350 μm.

polymer-well [29] or glass-well in a silicon substrate [30], and the formation of air within a substrate [31]–[33].

This paper discusses some of the aforementioned nontraditional TSV configurations, including their design, fabrication, and high-frequency measurements. In Section II, the integration of TSVs with microfluidic cooling is discussed. Section III presents coaxially shielded TSVs, which consist of multiple ground TSVs surrounding a signal TSV, benchmarked to other coaxial TSV technologies. Moreover, this section investigates the optimal number of ground TSVs to sufficiently shield a signal TSV. In Section IV, this paper discusses loss reduction techniques for TSVs in a silicon substrate.

II. TSVs INTEGRATED WITH MICROFLUIDIC COOLING

Fig. 1 illustrates three heterogeneous integrated microsystems with two cooling technologies (air and microfluidic). In Fig. 1(a), the logic and the memory dice are bonded side-by-side in a 2.5-D configuration with an air-cooled heat sink. Fig. 1(b) illustrates the integration of microfluidic cooling within a silicon interposer. Because microfluidic cooling offers a number of benefits compared to air cooling, significant reduction in junction temperature is expected in such systems. Fig. 1(c) illustrates a heterogeneous 3-D microsystem in which logic and memory dice are stacked on top of each other, with integrated microfluidic cooling. Such a 3-D stack can further improve bandwidth, latency, and I/O power because it provides the shortest interconnect lengths between chips. However, the 3-D stack has the highest integration complexity among the microsystems in Fig. 1.

Table I summarizes the specifications of TSVs integrated within microfluidic cooling technologies in the literature. One general challenge of such TSV integration is that it necessitates TSVs to be fabricated inside a microfluidic heat sink, and this introduces several fabrication challenges. From a cooling perspective, a relatively "thick" die is preferred since the height of a microfluidic heat sink is related to its cooling capability (thermal resistance) [16]. However, this inevitably requires TSVs to be relatively tall. For this reason, the height of most TSVs in Table I is more than 300 μm. On the other hand, from an electrical point of view, it is desired to have as small an allocation of copper as possible for TSVs in a silicon substrate. This is because the area allocated to copper TSVs directly consumes active circuit area. Moreover, as the diameter of TSVs increases, not only does electrical TSV capacitance increase, but thermomechanical stress also increases [34]. However, it should be noted that the diameter of TSVs cannot be boundlessly reduced since this will dramatically increase fabrication complexity, such as silicon etching and copper filling. Thus, it is critical to maximize the aspect ratio of TSVs without increasing fabrication complexity to satisfy both electrical and cooling metrics.

A. Fabrication of TSVs Embedded in a Silicon Microfluidic Heat Sink

Fig. 2 summarizes the fabrication process for TSVs embedded in a silicon microfluidic heat sink. The fabrication begins with the deposition of silicon dioxide followed by an anisotropic dry etch of the deposited oxide. Using the etched

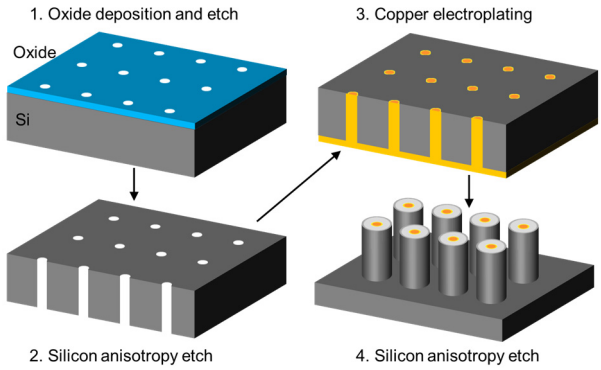


Fig. 2. Fabrication process of TSVs embedded in a silicon microfluidic pin-fin heat sink.

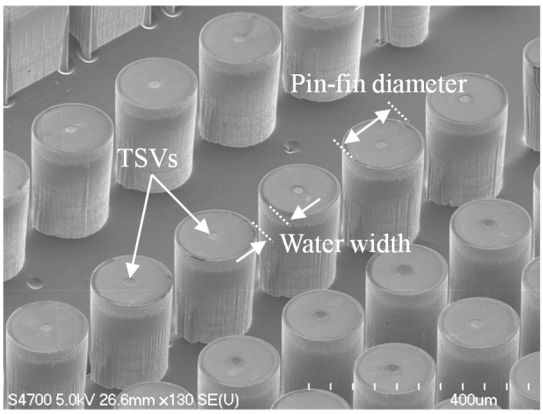
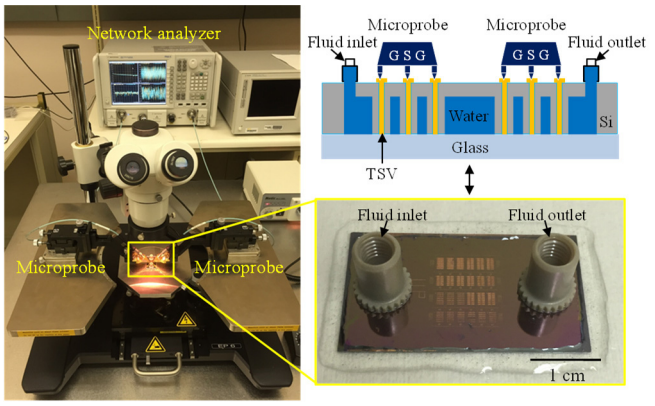
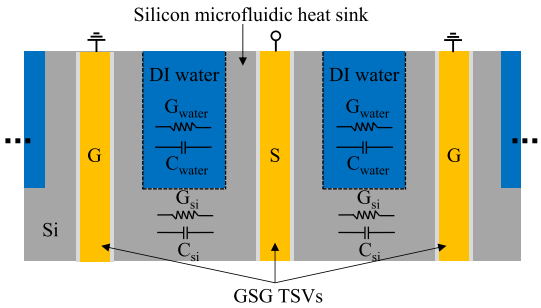


Fig. 3. SEM image of microfluidic pin-fins with embedded TSVs: Each pin-fin contains one TSV [19].



(a)



(b)

Fig. 4. (a) Measurement setup for the high-frequency characterization of the silicon pin-fin TSV testbed filled with DI water. (b) Schematic of GSG TSVs embedded in a silicon microfluidic pin-fin heat sink in the presence of DI water.

oxide as an etch mask, vias are etched in the silicon wafer using a deep reactive-ion etching process. After removing the remaining oxide, the wafer is placed in a thermal furnace at 1100 °C to form an oxide liner. Following thermal oxidation, electroplating is performed through three steps. First, a titanium and copper seed layer is deposited using an e-beam evaporator on the back side of the wafer. Second, dc electroplating is performed using an Enthone MICROFAB DVF electroplating solution to pinchoff the etched holes at the back side of the wafer. Next, a bottom–up electroplating process is performed to fill the etched holes with copper. After electroplating, removal of the excess copper is accomplished using chemical mechanical polishing (CMP) on both sides of the wafer. Finally, a circular microfluidic pin-fin structure is fabricated using the Bosch process, as shown in Fig. 3.

B. Frequency Response of TSVs With the Presence of Deionized Water

To evaluate the frequency response of TSVs in the presence of deionized (DI) water, the test bed is bonded (i.e., capped) to a glass wafer (to enable visualization) and filled with DI water, as shown in Fig. 4(a). To remove any undesirable conductivity in the DI water (such as ions), DI water with a conductivity of less than 0.5 μS/m and dissolved solid concentration of less than 0.5 ppm is chosen for the experiments. The high-frequency characterization of ground-signal-ground (GSG) TSVs is performed using microprobes and a network analyzer in the frequency range of 10–20 GHz. Prior to the measurements, short-open-load-through calibration is carried out on a calibration substrate. As shown in Fig. 4(b), there is a capacitive path partially through the DI water and the silicon between TSVs, and thus the frequency response of the GSG TSVs in the test bed is the aggregate S-parameters that include the electrical properties of both silicon and DI water.

Given that the permittivity of DI water varies from 78–11.5 in the frequency band of 1.8–57.8 GHz [35], this frequency-dependent permittivity of DI water may cause a large variation in TSV frequency response as a result of variations in TSV capacitance and conductance. First, the capacitance and conductance of TSVs in silicon are analyzed as a reference for our TSVs embedded in silicon pin-fins with DI water. As discussed in the literature [36], [37], the capacitance of TSVs is dominated by oxide capacitance at low frequency and saturates to the substrate (silicon) capacitance, as shown in Fig. 5 (left). Similarly, the conductance of TSVs is dominated by oxide conductance, which is nearly zero, at low frequency and saturates to the substrate (silicon) conductance, as shown in Fig. 5 (right). For the TSVs in silicon pin-fins with DI water, TSV capacitance is dominated by oxide capacitance at low frequency (similar to TSVs in silicon). However, at high frequencies, TSV capacitance is saturated

TABLE II
COMPARISON OF NONTRADITIONAL COAXIAL TSVS IN THE LITERATURE

Parameters	S. W. Ho et al. [21]	P. Thadesar et al. [24]	D. H. Jung et al. [22]	J.-M Yook et al. [23]	S. Adamshick et al. [25]	H. Oh et al. [26]
TSV diameter	100 μm	65 μm	30/42 μm (inner/outer)	70 μm	5 μm	13 μm
TSV height	300 μm	285 μm	205 μm	150 μm	50 μm	320 μm
Insulator material	SU-8	SU-8	ABF*	ABF	Silicon dioxide	Silicon dioxide
Insulator thickness	500 μm	125/150 μm (TSV pitch)	25 μm	20 ~ 120 μm (20 μm step)	0.5 μm	50/100 μm (TSV pitch)
Coaxial TSV formation	Photolithography	Photolithography	Laser ablation	Laser ablation	SACVD oxide	Silicon etch (Bosch process)
Note	RO4350B substrate used for the bottom chip	Multiple ground TSVs (instead of annular ground)	Two metal layers at top and bottom (sig. and gnd.)	High-R silicon substrate used for the bottom chip	Two metal layers at top and bottom (sig. and gnd.)	Isolation of TSVs from surrounding DI water

*ABF stands for Ajinomoto build-up film ($\varepsilon_r = 3.7$ and $tan\delta = 0.01$).

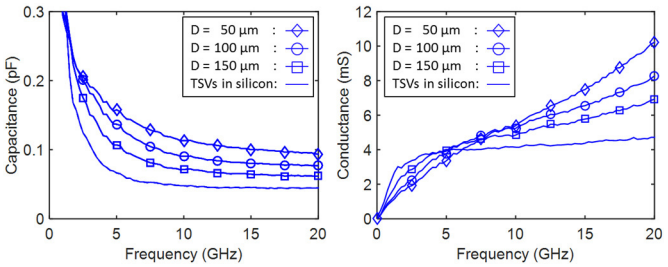


Fig. 5. Extracted capacitance and conductance from measurements. (D: the diameter of microfluidic pin-fins [19]. As D increases, spacing between the pin-fins is reduced.)

to the aggregate capacitance of both silicon and the high-permittivity DI water.

To quantitatively analyze this behavior, our test bed contains three pin-fin heat sink diameters (50, 100, and 150 μm) at a fixed TSV pitch of 200 μm. In other words, the width of the water region between the silicon pin-fins is 150, 100, and 50 μm, respectively, as shown in Fig. 3 (note, as the spacing increases, so does the volume of DI water between the signal/ground TSVs). Moreover, the test bed contains TSVs in a silicon substrate without any pin-fin structures as a reference. TSV capacitance and conductance are extracted from the measured S-parameters and shown in Fig. 5. As the diameter of pin-fins decreases, or equivalently the width of DI water region increases, TSV capacitance increases. This is due to the high permittivity of DI water compared to the permittivity of silicon. At 20 GHz, the capacitance of TSVs in microfluidic pin-fins with DI water is 91.5, 76.9, and 62.0 fF when the diameter of the pin-fins is 50, 100, and 150 μm, respectively; the capacitance of TSVs in silicon is 44.76 fF. However, the measured TSV conductance shows the opposite behavior at low- and high-frequency ranges. At a low-frequency range, TSV conductance decreases as the volume of DI water between TSVs increases, or the diameter of pin-fin decreases. At a high-frequency range, TSV conductance increases as the volume of water increases. At 20 GHz, the conductance is 10.4, 8.3, and 6.9 mS when the diameter of the pin-fins is 50, 100, and 150 μm, respectively, and TSV conductance is 4.7 mS for the reference TSVs in silicon.

III. COAXIALLY SHIELDED TSVS WITHIN A MICROFLUIDIC PIN-FIN HEAT SINK USING A COAXIAL CONFIGURATION

As discussed in Section II, the frequency-dependent permittivity of DI water significantly impacts the electrical characteristics of GSG TSVs. To mitigate this issue, this section discusses electrically shielded TSVs for liquid-cooled microsystems. In general, to shield undesirable noise or coupling, a coaxial configuration is utilized. For integrated microsystems, coaxial TSVs have been proposed to shield vertical signal transmission in a silicon substrate [21]–[26], as summarized in Table II. The coaxial TSVs show good shielding performance, as well as reduced noise and loss. However, they face a number of fabrication challenges. First, the fabrication of a coaxial structure requires additional materials or processes, such as SU-8 [21], [24], ABF [22], [23], or oxide using SACVD [25]. Moreover, the outer ground conductor of the coaxial TSVs is typically larger in area than the center signal TSV. This is because the ground conductor is annular, while the signal via is circular; this geometry and size mismatch increases fabrication complexity in the Bosch process as well as in electroplating.

To address these challenges without increasing fabrication complexity, this section describes a coaxial-like concept to shield a signal TSV by placing multiple ground TSVs (instead of an annular conductor) around the center signal TSV, as shown in Fig. 6(a). Such an approach enables the wafer-level batch fabrication of signal and ground TSVs simultaneously. Fig. 6 illustrates the layout and measurement setup of coaxially shielded TSVs with their dimensions. It is expected that there is an optimal number of ground TSVs to sufficiently shield the signal TSV. To analyze this behavior, the coaxially shielded TSVs in the test bed consist of a number of ground TSVs (0, 1, 2, 4, 6, and 8). Fig. 7(a) shows an X-ray image of coaxially shielded copper TSVs with a varying number of

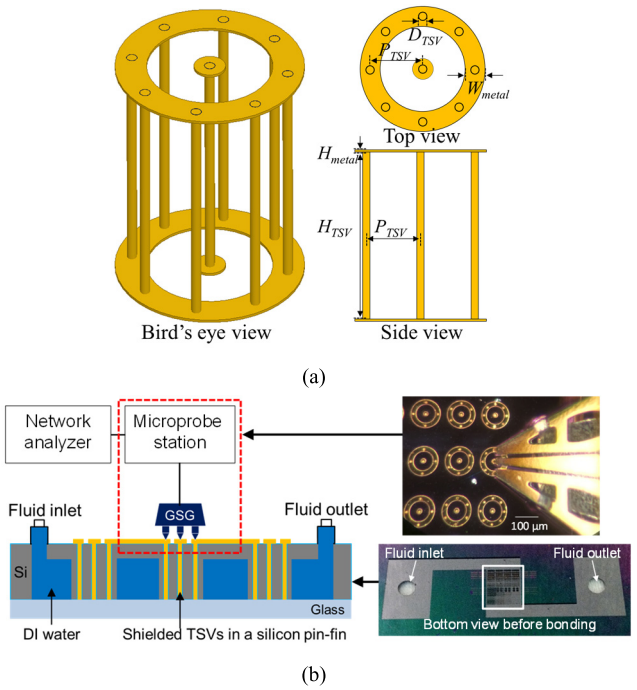


Fig. 6. (a) Layout of the coaxially shielded TSVs using multiple (0, 1, 2, 4, and 8) ground TSVs: $D_{\mathrm{TSV}} = 13\ \mu$m, $H_{\mathrm{metal}} = 3\ \mu$m, $H_{\mathrm{TSV}} = 320\ \mu$m, $W_{\mathrm{metal}} = 20\ \mu$m, and $P_{\mathrm{TSV}} = 50$ and $100\ \mu$m. (b) Measurement setup for the high-frequency characterization of the TSV test bed filled with DI water.

ground TSVs. To facilitate probing, annular-shaped metal pads are selectively deposited to short all ground TSVs, as shown in Fig.7(b).

To investigate the frequency response of the coaxially shielded TSVs, the fabricated test bed is bonded to a glass substrate (to encapsulate the fluidic passages) and filled with DI water, as illustrated in Fig. 6(b). In our high-frequency measurements, single-port characterization is performed since TSV capacitance and conductance can be directly extracted from a scattering matrix [36], [37]. In this paper, we focus on evaluating the variation in terms of the magnitude and phase of the scattering matrix for the shielded and nonshielded TSVs. Fig. 8 illustrates the measured S_{11} values for both the shielded and nonshielded TSVs. For each case, two sets of measurements are performed in the following manner. First, we measure the S-parameters of the TSVs in a silicon substrate ("TSVs in silicon" in Fig. 8). Next, we perform another measurement for the TSVs within a microfluidic pin-fin heat sink surrounded by DI water ("TSVs in water" in Fig. 8). For the nonshielded TSV case, a maximum of 1.46 dB difference is found between TSVs in silicon and the TSVs in microfluidic pin-fins with water. However, for the shielded TSVs, the magnitude difference was suppressed to 0.08 dB, and the phase variation was also significantly suppressed. The capacitance and conductance of TSVs in both cases are extracted from the measurements, as shown in Fig. 9. The results show a maximum difference of 0.14 pF in capacitance and 2.75 mS in conductance for nonshielded TSVs, while these are reduced to 0.02 pF and 1.12 mS, respectively, with the shield TSVs. This clearly indicates that signal transmission in the shielded TSVs is mostly isolated despite the presence of DI water.

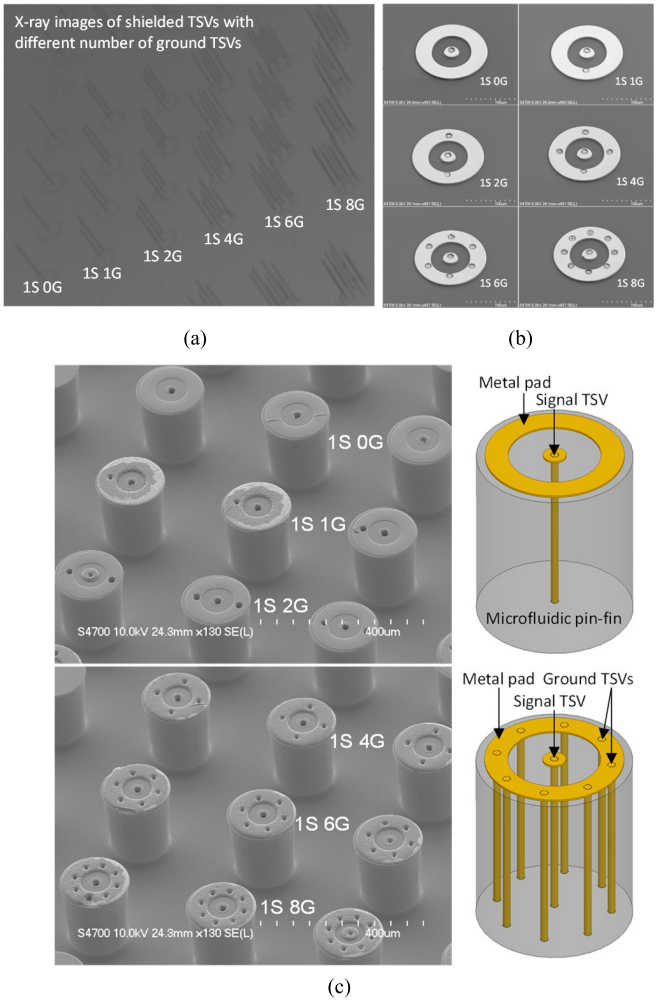
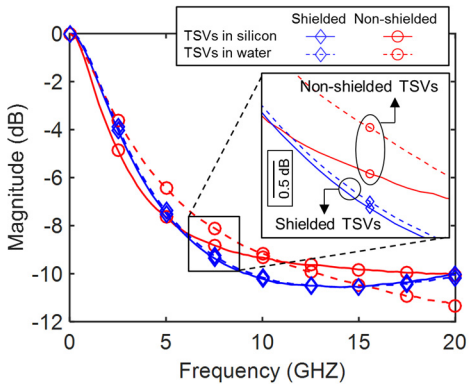


Fig. 7. (a) SEM images of TSVs with the metal pad connecting ground TSVs (a front side view). (b) X-ray images of a TSV array with different numbers of ground TSVs (0, 1, 2, 4, 6, and 8 ground TSVs). (c) Schematics and SEM images of microfluidic pin-fins with different number of ground TSVs (a back side view). A signal TSV is located at the center surrounded by ground TSVs.

TABLE III
MAXIMUM VARIATION OF MAGNITUDE AND PHASE WITH RESPECT TO THE NUMBER OF SURROUNDING GROUND TSVS

	Non-shield	Coaxially-shielded TSVs				
	1S 0G	1S 1G	1S 2G	1S 4G	1S 6G	1S 8G
Mag. (dB)	1.46	0.56	0.46	0.32	0.21	0.08
Phase (deg)	14.42	13.88	10.03	7.79	8.54	6.84

To quantitatively analyze this shielding effect with respect to the number of ground TSVs, five sets of shielded TSVs are measured, as summarized in Fig. 10 and Table III. First, the nonshielded TSVs are measured as a reference, showing a maximum magnitude difference of 1.46 dB between the silicon and microfluidic heat sink cases. It can be seen that the measurement variation reduces both in magnitude and phase as the number of ground TSVs increases. The results clearly indicate that the shielded TSVs with eight ground TSVs almost preserve TSV frequency response regardless of surrounding medium. However, as the number of ground TSVs increases, the allocation for copper in silicon increases. As discussed



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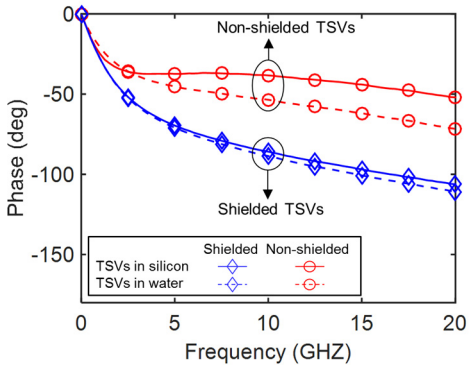


(b)

Fig. 8. High-frequency measurement results. (a) Magnitude and (b) phase of S_{11} of coaxially shielded and nonshielded TSVs in silicon and DI water, respectively.

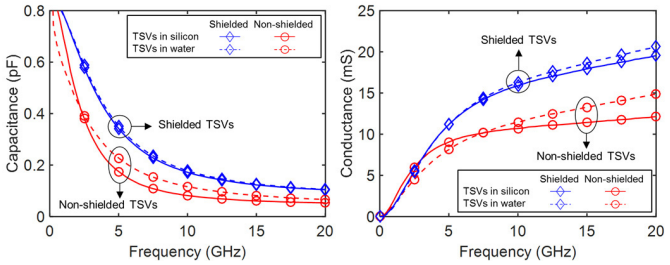


Fig. 9. Extracted capacitance and conductance from measurements for coaxially shielded and nonshielded TSVs.

in Section II, it is preferable to minimize the allocation of copper in a silicon substrate. Thus, it is critical to determine the optimal number of ground TSVs that provides sufficient shielding. In our measurements, four to six ground TSVs showed sufficient shielding.

IV. Low-Loss TSV Technology

To attain a significant reduction in TSV electrical loss, various approaches have been studied (as summarized in Table IV). Low-k materials and increased liner thickness were proposed to reduce capacitance and loss [27]. To reduce substrate losses at a higher frequency range, high-resistivity silicon and glass substrates were proposed [27], [28]. Moreover, instead of changing an entire substrate, several

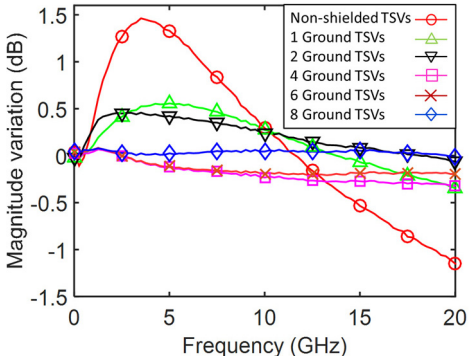
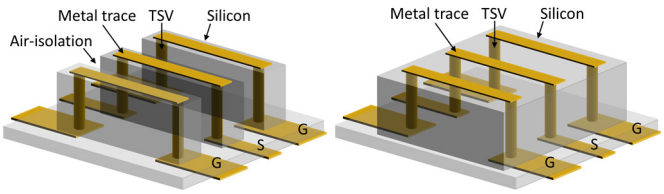


Fig. 10. Magnitude variation of nonshielded TSVs and shielded TSVs with different number (0, 1, 2, 4, 6, and 8) of ground TSVs.



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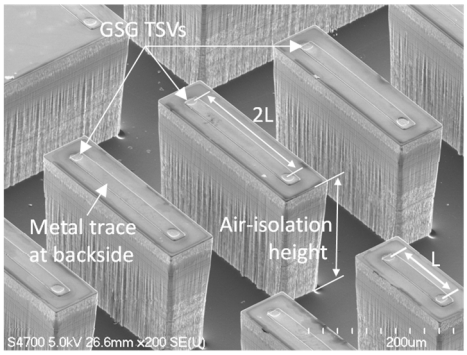

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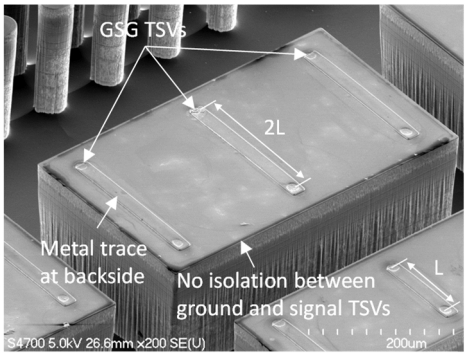

(c)

Fig. 11. (a) 3-D schematics of air-isolated TSV technology (left) and nonisolated TSVs (right) with a GSG configuration. SEM images of (b) air-isolated TSVs and (c) nonisolated TSVs. Etched silicon with back metal traces of a length of L and 2L, respectively.

researchers have proposed the substitution of a localized silicon region with low-loss materials. One study proposed the formation of local polymer-wells with embedded TSVs in a silicon substrate [29]. In a similar manner, localized glass

TABLE IV
COMPARISON OF NONTRADITIONAL TSVS FOR ELECTRICAL LOSS REDUCTION IN THE LITERATURE

Parameters	P. Thadesar et al. [29]	J.-Y. Lee et al. [30]	V. Sukumaran et al. [28]	M. Sunohara et al. [31]	H. Oh et al. [32]	C. Huang et al. [33]
TSV diameter	65/100 μm	40 μm	15 μm (upper**) 7~8 μm (lower)	60 μm	13 μm	10/30 μm
TSV height	285 μm	100 μm	30 μm	350 μm	300 μm	50 μm
TSV pitch	250 μm	80/90/100 μm (TSV spacing)	27 μm	200 μm	100 μm	N/A
Low-loss technique	Localized SU-8 into silicon	Localized glass into silicon	Glass substrate	Air trench between silicon and copper	Air isolation in silicon	Air gap between silicon and copper
Low-loss formation	SU-8 fill after silicon etch	Glass reflow after silicon etch	Glass substrate	Silicon etch (width: 20~30 μm)	Silicon etch (width: 50 μm)	PPC*
Insertion loss	~1 dB @ 50 GHz	~0.4 dB @ 50 GHz	~0.1 dB @ 20 GHz	~6.2 dB @ 40 GHz	~0.5 dB @ 20 GHz	N/A
Characterization	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	De-embedded single TSV loss	DC capacitance measurements

*PPC stands for propylenecarbonate.
**Tapered TSVs are shown with the dimension of 15 μm at one end and 7~8 μm at the other end.

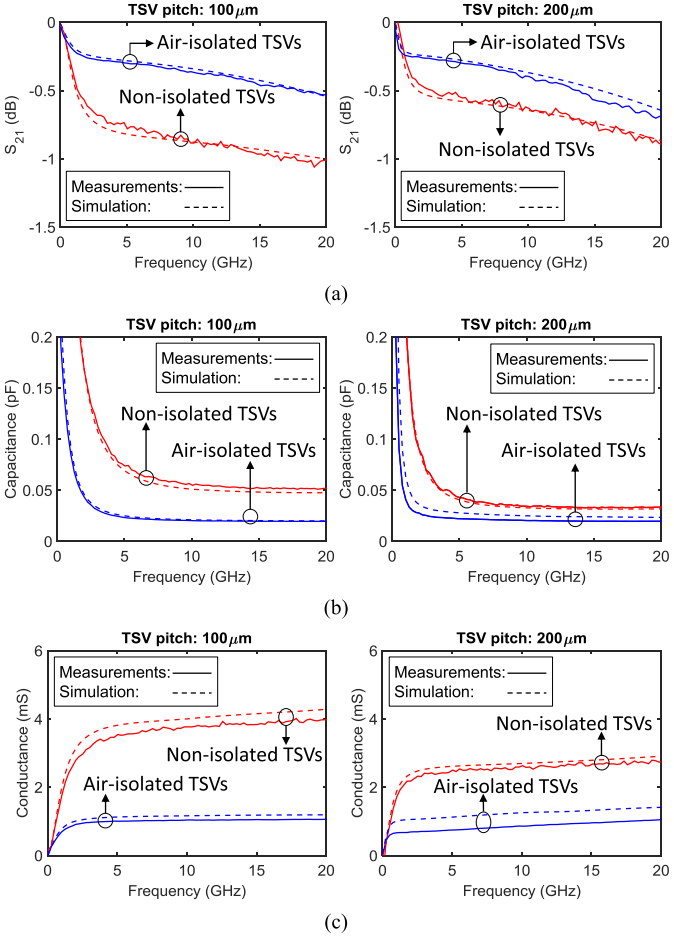

Fig. 12. (a) Insertion loss of air-isolated and nonisolated TSVs for TSV pitches of 100 and 200 μm after L-2L deembedding. (b) Extracted TSV capacitance. (c) TSV conductance from the measured scattering matrixes.

formation was demonstrated using glass reflow after partially etching a silicon substrate [30]. In addition, the formation of an air gap between copper and silicon was proposed using propylenecarbonate [33] or air trench formation [31]. The permittivity of air is approximately 1, and thus it is most attractive to use air for loss reduction. However, the fabrication of an air liner or air gap between copper and silicon is considered challenging since it requires additional materials and fabrication steps.

To address such challenges, this section discusses low-loss TSVs achieved by simply etching silicon around the TSVs for silicon interposer applications [32]. This approach results in reduced loss, as well as capacitance of TSVs, while avoiding complex fabrication steps.

Fig. 11 presents the two types of GSG TSVs embedded in silicon pillars with 3-D layouts and SEM images. Fig. 11(b) shows air-isolated TSVs, where signal and ground TSVs are partially isolated using air. On the other hand, the GSG TSVs in Fig. 11(c) do not include any isolation between signal and ground TSVs, which we refer to as nonisolated TSVs. To investigate the reduction in insertion loss and TSV parasitics, the fabricated air-isolated and nonisolated TSVs are compared using high-frequency measurements and full-wave simulations. To extract single TSV loss from a TSV/trace-mixed structure, the L-2L deembedding technique [38] is performed using two lengths (L and 2L as shown in Fig. 11) of metal traces. The height and width of the air-isolation are 220 and 50 μm, respectively. TSV diameter and height are 13 and 320 μm, respectively, and TSV pitches of 100 and 200 μm are used. Fig. 12 illustrates the insertion loss, extracted capacitance, and conductance of single TSV after L-2L deembedding. It shows approximately 50% and 30% reduction in insertion loss at 20 GHz for the TSV pitch of 100 and 200 μm, respectively.

V. CONCLUSION

This paper discusses the design considerations, fabrication, and high-frequency characterization of three types of nontraditional TSV technologies. First, TSVs integrated with

microfluidic cooling are discussed for thermally limited 3-D integrated microsystems. This paper investigates the impact of microfluidic designs on TSV electrical performance since the frequency-dependent permittivity of DI water significantly changes TSV electrical parasitics. The capacitance and conductance of TSVs increased by 104.4% and 121.3%, respectively. This implies that the design of microfluidic cooling is strongly correlated with electrical TSV performance, and vice versa. Second, coaxial TSV configurations were investigated to electrically shield signal transmission in TSVs. Coaxially shielded TSVs, in which multiple ground TSVs surround a signal TSV, successfully shielded signal TSVs from the impact of the surrounding DI water. While shielding improves as the number of ground TSV increases, it also increases the area allocation of copper in a silicon substrate. Thus, an optimal number of ground TSVs should be considered to satisfy shielding requirements, minimize silicon real estate, and lower manufacturing cost. Finally, low-loss TSV techniques were discussed for silicon interposer applications. While there are many loss-reduction techniques in the literature, air-isolation in a silicon substrate greatly reduces the electrical loss and capacitance of TSVs without increasing fabrication complexity.

ACKNOWLEDGMENT

The authors would like to thank technical staff with the Institution of Electronics and Nanotechnology (IEN), Georgia Tech. They would also like to thank Enthone for providing electroplating solutions and Cabot Microelectronics Corporation for providing CMP slurries.

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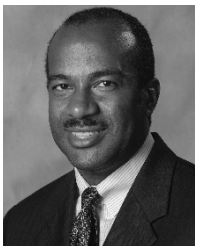

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